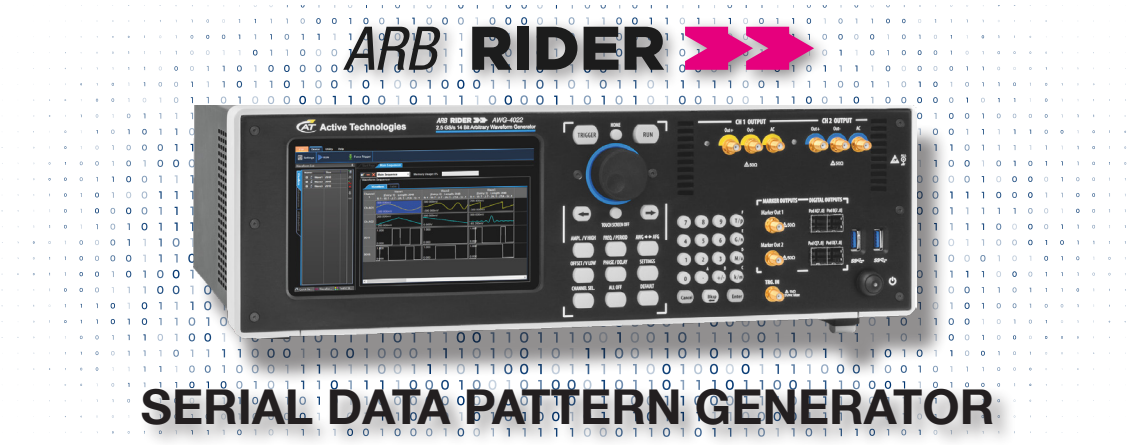
How To Characterize Digital Logic with the AT-AWG-4010 Series Serial Data Pattern Generator

APPLICATION NOTE



Introduction

This document describes how to use the AT-AWG-4010 Series Serial Data Pattern Generator to generate the signals for the test and the characterization of standard logic gates and all generic digital systems. The AT-AWG-4010 Series Serial Data Pattern Generator simplifies the multilevel pulse generation thanks to its features that combine the pulse and edge shaping with the ability to reproduce a multilevel programmed pattern.
Considering the amplitude of 12 Vpp into 50 Ohm (24 Vpp into open) joined to an analog shift of ±6 V into 50 Ohm (±12 V into open) and the maximum symbol rate of 300 Mega-Symbols per second, this instrument finds application also as a replacement of discontinued products like the Agilent 81110A series.

Key Issues:

- Characterize digital logic gates and integrated circuits.

Solutions:

- AT-AWG-4012/4014/4018 Serial Data Pattern Generator

Results:

- Accelerate research, reliability and failure analysis studies of semiconductor devices.
- Reduce the time from setup to running characterization of digital logic gates

Active Technologies

AT-AWG-4010 SPG Key Features

Up to 4 logic levels

For each channel it is possible to define up to 4 independent voltage levels to emulate, in addition to logic '0' and '1', a tristate buffer or a weak '0' signal when a bus is not driven.

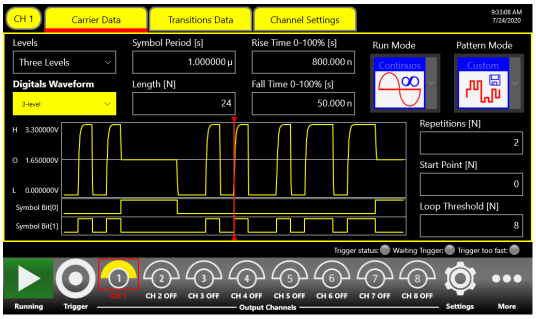


Figure 1: User interface with level settings

Edge Definition

The shape of each transition between the levels can be arbitrarly defined by the user. You can use this feature to shape the edge as RC transient or to add a positive overshoot. The 14 bit DAC resolution and the 318 MHz analog bandwidth provides you an excellent signal fidelity.

Amplitude

The AT-AWG-4018 Serial Data Pattern Generator can reach up to 12 Vpp amplitude into 50 Ohm (24 Vpp into open); furthmore it is available a programmable hardware offset (called baseline offset) that allows shifting the voltage window of ±6 V into 50 Ohm (±12 V into open).
In this way by using the baseline offset, the instrument can generate a 0 - 12 V signal into 50 Ohm (0 - 24 V into open).

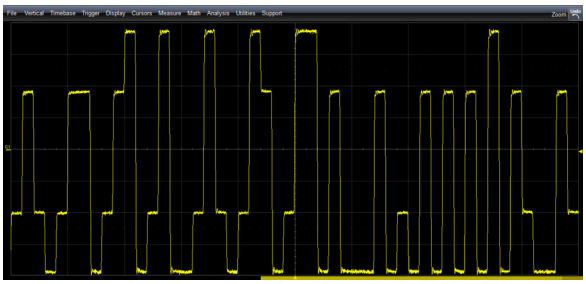


Figure 2: Multi Level Pattern

Multi-Instrument synchronization up to 32 channels

Each unit has 8 independent analog channels and it is possible to synchronize up to 4 units to build a 32-channels system.

Fine time resolution

Thanks to advanced signal processing, the skew between the channels can be controlled with a resolution in the order of 1 ps.

Generation Modes

- **Continuous**: the generation starts when the user presses the Start button and it ends when the user presses the stop button.
- **Burst**: the instrument waits for a trigger and then the pattern is generated for the selected number of times. At the end of the burst the instrument waits for a new trigger.
- **Modulation**: the instrument applies a AM, FM, PM, FSK or PSK modulation to the generated pattern.

Selectable Header

The memory depth allows a pattern length up to 2 Mbits, but it is possible to select an initial part of the total pattern that is generated once while the rest of the pattern is repeated more times.

Intuitive User Interface

The user interface allows you to easily program the instrument, using the touch screen and the physical keyboard. If you need to integrate the instrument into an automatic testbench, the AT-AWG-4010 Series Data Pattern Generator can be controlled by an external controller via SCPI command.

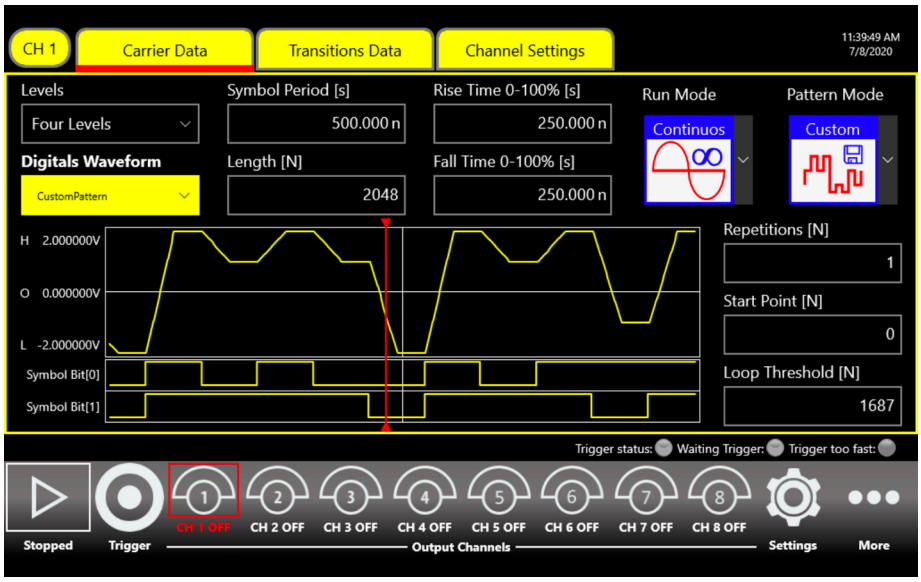


Figure 3: Serial Pattern Generator User Interface

Standard Logic Gates

Standard logic gates are the basic logic blocks that compose all the digital circuits.
Although nowadays the development of digital applications is realized through programmable IC such as MCU (MicroController Unit) or PGA (Programmable Gate Array), the discrete gates still find applications when the designers need a function that can't be realized directly in the programmable IC or if the application is not enough complex to include a programmable IC on the board.
In some cases, it is necessary to add external logic gates to reach a bit rate that a programmable device can not support or to insert a level shifter to allow the communication between IC with different voltage standards or to insert a multiplexer to increase the number of pins of a MCU.

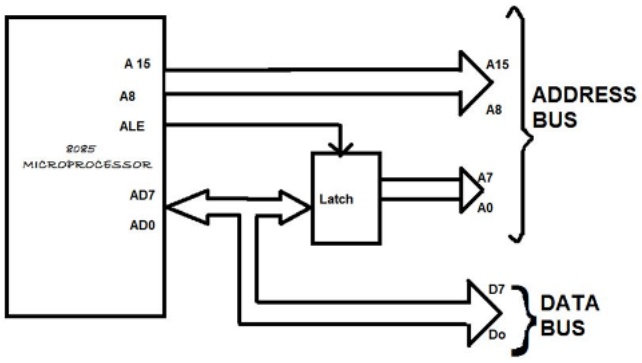
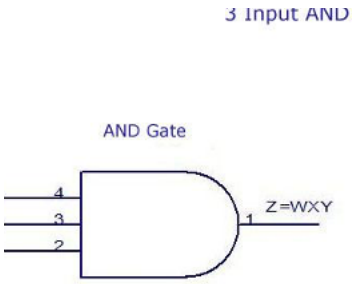


Figure 4: De-multiplexing of address/data bus using an external latch

There are many types of devices from different logic families (TTL, CMOS, BiCMOS, etc.) with the same logical function.
To characterize and test them, from the simplest ones such as the single gates (NOT, NAND, NOR, and so on) to the more complex ones such as multichannel latches and counters, it is necessary to generate signals with specific characteristics in term of edge shaping, overshoot, amplitude, etc.
Indeed it is necessary to remember that the digital signals are not ideal, but since we are in the real world, they take a bit of time to switch and can be affected by overshoot, so the right test signal is an analog signal that allows you to test a specific feature.
For all those applications, the AT-AWG-4010 Series Serial Data Pattern Generator is the perfect solution, because you can combine the digital pattern with the analog characteristics like edge shaping, amplitude, noise, modulation of the analog front end.
In the following section we will illustrate how to generate the signals needed for the digital tests with the Serial Data Pattern Generator, as example we report a typical application.

A. Measurement of the Propagation Delay of Asynchronous Logic Gate

For this application we will consider a 3 input AND gate, but the topic remains valid for every logic network. It is known that the 3 inputs of the AND gate are logically equivalent, but the analog characteristics such as the propagation delay depends on the internal architecture.



TRUTH TABLE

INPUTS			OUTPUT
W	X	Y	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Figure 5: : Symbol and truth table of a 3 input AND gate

Using the AT-AWG-4010 Series Serial Data Pattern Generator, you are able to define analog characteristics of the signals on each input of the gate under test, setting the voltage level and the edge shaping independently among the channels.

In the pictures below you can see the connections for this test:

- The channel 1, 2, 3 of the pattern generator are connected to the input of the AND gate.
- The channel 4 is connected to oscilloscope as reference.
- The Output of the AND gate is connected to the oscilloscope.
- For simplicity the power supply, the ground and other components needed for the proper operation of the AND gate has been omitted.

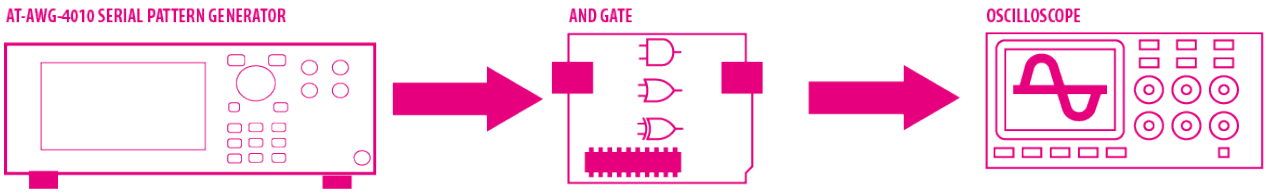


Figure 6: Set up for asynchronous logic gates characterization

Now let's look at how to configure the Pattern Generator using the software interface.

1. From Carrier Data tab, set the level number to 2, define the bit rate and select Custom as Pattern Mode.

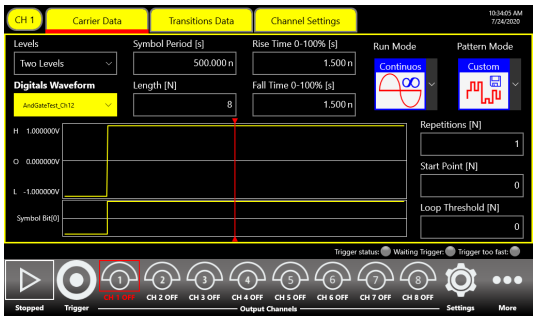


Figure 7: Carrier Data Page

2. From the "Transition Data" tab, define the shape of the edges; in this case we set as linear defining a rise/fall time of about 4 ns. Define the levels by setting the voltage levels of each transition.

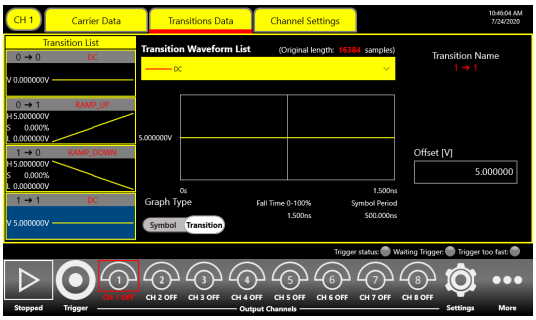


Figure 8: Transition Data Page

4. Definition of the pattern:
   Ch 1: 01111111
   Ch 2: 01111111
   Ch 3: 00011110
   Ch 4: 00011110
   Ch 5 – 8: not used

   Since we want to evaluate the propagation delay of the input 3, the input 1 and 2 go to high level at the same time and when they are stable, the input 3 executes the rising edge, stays at high level for 4 symbols and then executes a falling edge. The channel 4 behavior is the same of the channel 3 and it is used as reference for the oscilloscope.

Figure 11: Import Page

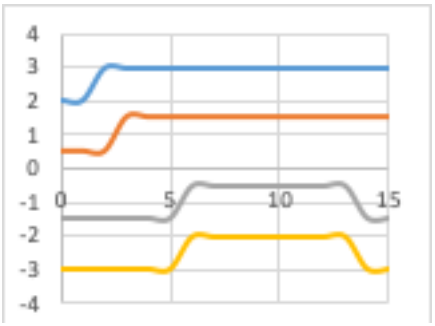


Figure 10: Diagram of the programmed pattern

5. Press the Run button and observe the results.

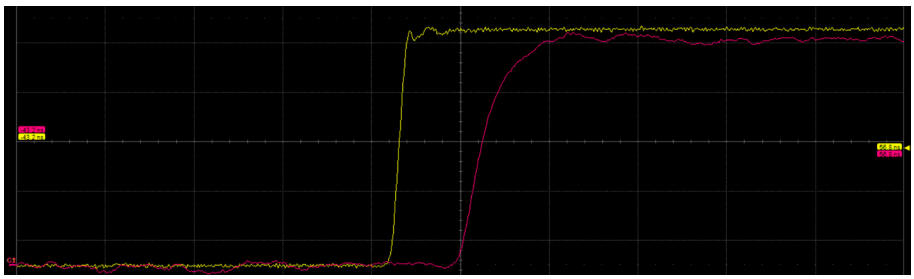


Figure 12: Oscilloscope screen with the result of the test

In the oscilloscope screenshot above, we can observe delay between the output of the logic gate and the channel 4 of the SPG.

Note: to compensate the delay of the cables you can adjust the initial delay of the channel 4. This setup is useful to characterize the input-to-output propagation delay for the input 3, but by changing the pattern you can observe also the behavior of other inputs.

B. Effects of Simultaneous Switches in Asynchronous Logic Gate

Working with asynchronous logics, it can be interesting to investigate the behavior of the logic gate at the simultaneous switch of two or more inputs. So starting from the previous set-up, we want to test what it happens if the input 1 goes at high level while the input 2 goes at low level.

Now we load the following pattern:
Ch 1: 11000011
Ch 2: 00111100
Ch 3: 11111111
Ch 4 – 8: not used

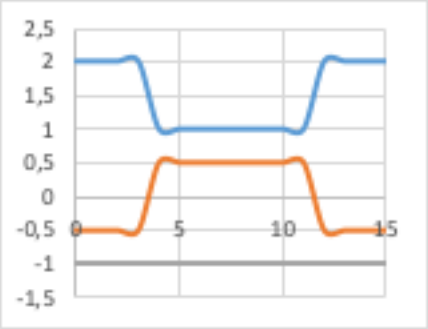


Figure 13: Diagram of the programmed pattern

Logically the output should be always '0', but depending on the edges of the input signal and on the internal architecture of the logic gate under test, it is possible to see a spike on the output. In the pictures below you can see that, although the output should be always 0, there are 2 spikes at the input switches.

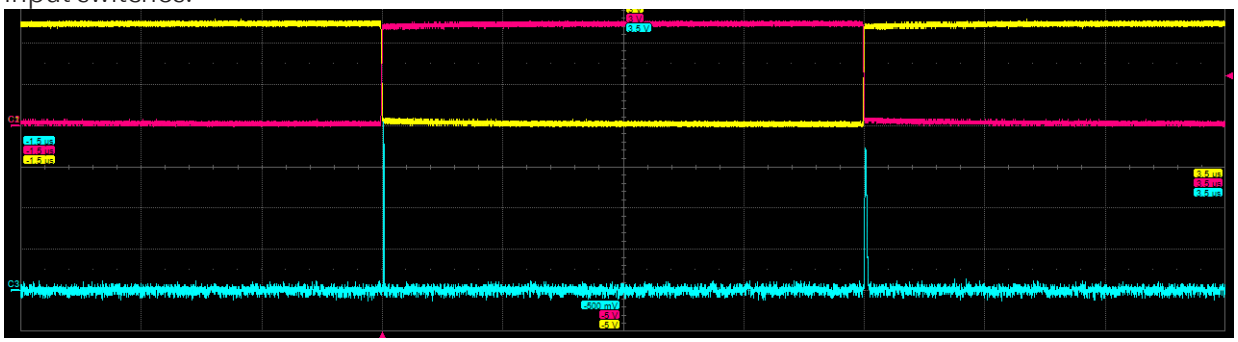


Figure 14: Oscilloscope screen with the result of the test

To summarize, below we report the oscilloscope screenshot about other tests, obtained by varying the rise/fall time and the skew between the channels.

- Skew channel 1 – 2: 2 ns
- Rise / Fall time: 4 ns

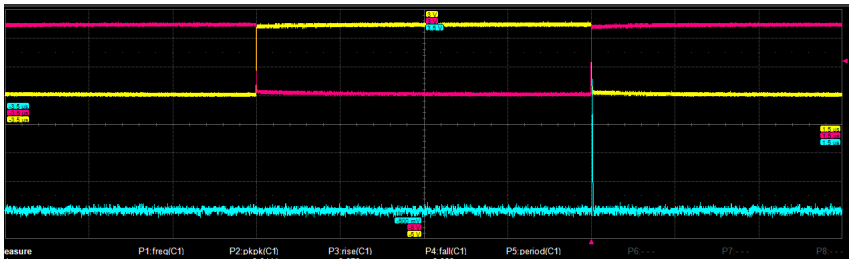


Figure 15: Oscilloscope screen with the result of the test

As you can see in the picture above, adding a skew on the output appear a spike when the input 1 switches to high level.

- Skew channel 1 – 2: 0
- Ch 1 Rise time 7 ns
- Ch 1 Fall time 4 ns
- Ch 2 Rise time 7 ns
- Ch 2 Fall time 4 ns

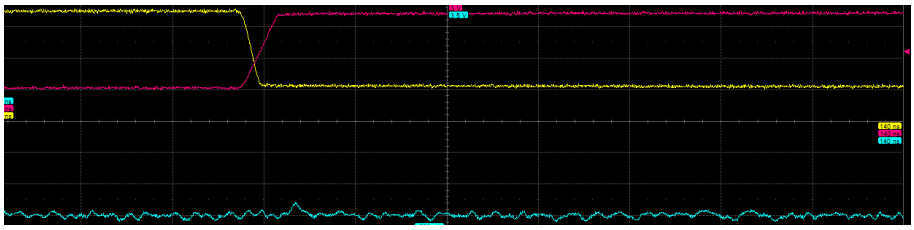


Figure 16: Oscilloscope screen with the result of the test

As you can see in the picture above, with those settings there is not any spike.

Conclusion

The AT-AWG-4010 Series Data Pattern Generator offers you a set of tools to address the most complex applications on digital devices characterization.
Multiple outputs, high voltage window, custom and modulated pattern generation are unique features that can help designers to test with confidence their devices under test; the ease to use user interface allows you to simplify and speed up the setup of your most complex systems.

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About Us

Active Technologies was founded in 2003 as start-up of the University of Ferrara, in Italy, and immediately involved in large EU research experiments, mostly vs semiconductor test and innovative instrumentation design.
The company mission is to deliver the industry's best signal stimulus solution as fast pulse generator, arbitrary waveform generator and digital pattern generator.

The research group works in a close cooperation with physics and academic research centers, semiconductor and automotive industries, in order to deliver the state of the art solution for signal testing.

The cooperation and the OEM projects with top Test and Measurement players in the world proofs the unique features and the flexibility of the technologies developed into the company.

As a Small Medium Enterprise (SME), Active Technologies can be involved in EU research projects to customize a specific test solution.
So far Active Technologies has already joined 8 EU projects under FP7, H2020 and ECSEL programs.

All Products are designed and manufactured in Italy (100% MADE IN ITALY PRODUCTS)

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